the second conductor layer having wiring patterns therein;

wherein one or more of the wiring patterns of the first conductor layer and the second conductor layer are electrically connected to the at least one semiconductor element imbedded in the first insulating layer and the at least one semiconductor element imbedded in the second insulating layer.

Cont'd B2

REMARKS

In accordance with the foregoing, claim 1 has been amended and claims 14-17 have been added. Claims 1-6 and 14-17 are pending and under consideration.

OBJECTION TO THE DRAWINGS

At page 2 of the Office action, the Examiner pointed out that Figures 1A-1D should be labeled as prior art. Accordingly, a proposed drawing correction to FIGS. 1A-1D together with corrected formal drawings are provided herein together with a request to enter the corrected formal drawings.

REJECTION UNDER 35 U.S.C. 102

At page 2 of the Office action, the Examiner alleges that Kim et al. disclose "a plurality of insulating layers located on and above the surface thereof...; conductor layers having wiring patterns formed therein and located on the insulating layer...; semiconductor elements...imbedded and mounted inside the insulating layer wherein the wiring patterns are mutually electrically connected..., passing though the insulating layers and the semiconductor elements are electrically connected to the wiring patterns...and wherein two or more semiconductor elements are imbedded and mounted inside each of said plurality of insulating layers (figure 5C)."

Applicants respectfully submit that Kim et al. is directed to, and limited to, a stackable semiconductor package having a non-conductive substrate main body having a plurality of patterned conductive wires formed therein, and a cavity to receive a semiconductor chip. Accordingly, it is respectfully submitted that Kim et al. does not teach or suggest, among other

things, "plural pairs of conductor layers having wiring patterns and an insulating layer located thereon, wherein; a semiconductor element is imbedded inside said insulating layer; the semiconductor element is electrically connected to a wiring pattern of said conductor layer; and a wiring pattern of said conductor layer is electrically connected, by via holes, to a wiring pattern of the conductor layer of a different pair of a conductor layer having wiring patterns and an insulating layer located thereon," as recited in independent claim 1, as amended.

For at least the reasons that Kim et al. does not teach each feature as recited in independent claim 1 of applicants' invention, this patent cannot be used to properly anticipate this claim. Accordingly, it is respectfully submitted that independent claim 1, as amended, is patentable over Kim et al., and withdrawal of this rejection and allowance of independent claim 1 are earnestly solicited.

Further, for at least the reason that claims 2-6 depend from allowable independent claim 1, and that Itabashi et al. is used by the Examiner for the limited purpose of providing the teaching of electrically connecting a wiring pattern to a semiconductor element by flip chip mounting, and does not teach or suggest the features listed supra which are recited in independent claim 1, as amended, and are also missing from Kim et al., it is respectfully submitted that these claims are also allowabie over Kim et al.

Applicants respectfully submit that new claims 14 and 17 are also allowable over Kim et al. since this patent does not teach or suggest, "a first insulating layer; a first conductive layer having wiring patterns formed under the first insulating layer; a second conductive layer having wiring patterns formed over the first insulating layer, one or more of the wiring patterns of the second conductive layer being electrically connected to one or more of the wiring patterns of the first conductive layer through via holes; and at least one semiconductor element imbedded inside the first insulating layer and electrically connected to at least one of the wiring patterns of the first conductive layer and at least one of the wiring patterns of the second conductive layer," as recited in new independent claim 14, or "a first insulating layer formed over a first conductor layer, the first insulating layer having at least one semiconductor element imbedded therein and the first conductor layer having wiring patterns therein; and a second insulating layer formed over a second conductor layer, the second insulating layer and conductor layer being formed over the first insulating layer and first conductor layer, the second insulating layer having at least one semiconductor element imbedded therein and the second conductor layer having wiring patterns therein; wherein one or more of the wiring patterns of the first conductor layer

and the second conductor layer are electrically connected to the at least one semiconductor element imbedded in the first insulating layer and the at least one semiconductor element imbedded in the second insulating layer," as recited in new independent claim 17.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: Sept 18, 2002

By: _____
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please AMEND the following claims:

1. (ONCE AMENDED) A semiconductor device comprising:

[a base substrate on one surface of which wiring patterns are formed;

a plurality of insulating layers located on and above said surface thereof;]

plural pairs of conductor layers having wiring patterns [formed therein and located on the insulating layers;] and an insulating layer located thereon

[semiconductor elements imbedded and mounted inside the insulating layers]; wherein:

[said wiring patterns are mutually electrically connected, passing through said insulating layers; and

said semiconductor elements are electrically connected to said wiring patterns]

a semiconductor element is imbedded inside said insulating layer;

the semiconductor element is electrically connected to a wiring pattern of said conductor layer; and

a wiring pattern of said conductor layer is electrically connected, by via holes, to a wiring pattern of the conductor layer of a different pair of a conductor layer having wiring patterns and an insulating layer located thereon.

Please ADD the following claims:

14. (NEW) A semiconductor device comprising:

a first insulating layer;

a first conductive layer having wiring patterns formed under the first insulating layer;

a second conductive layer having wiring patterns formed over the first insulating layer, one or more of the wiring patterns of the second conductive layer being electrically connected to one or more of the wiring patterns of the first conductive layer through via holes; and

at least one semiconductor element imbedded inside the first insulating layer and electrically connected to at least one of the wiring patterns of the first conductive layer and at least one of the wiring patterns of the second conductive layer.

15. (NEW) The semiconductor device according to claim 14, further comprising a second insulating layer having at least one semiconductor element imbedded therein, the second insulating layer being separated from the first insulating layer by one of the first and second conductor layers, and the at least one semiconductor element of the second insulating layer being electrically connected to one or more of the wiring patterns of the first and second conductor layers.

16. (NEW) The semiconductor device according to claim 14, wherein one or more of the wiring patterns of the first conductor layer are electrically connected to one or more of the wiring patterns of the second conductor layer.

18. (NEW) A semiconductor device comprising:

a first insulating layer formed over a first conductor layer, the first insulating layer having at least one semiconductor element imbedded therein and the first conductor layer having wiring patterns therein; and

a second insulating layer formed over a second conductor layer, the second insulating layer and conductor layer being formed over the first insulating layer and first conductor layer, the second insulating layer having at least one semiconductor element imbedded therein and the second conductor layer having wiring patterns therein;

wherein one or more of the wiring patterns of the first conductor layer and the second conductor layer are electrically connected to the at least one semiconductor element imbedded in the first insulating layer and the at least one semiconductor element imbedded in the second insulating layer.

CERTIFICATE UNDER 37 CFR 1.8(a)
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231
on September 18, 2002
STAAS & HALSEY
By: [signature]
Date: September 18, 2002